

AMENDMENT TO THE CLAIMS

Please enter new claims 24-43 in this application. No new matter is believed to be entered as a result of these new claims.

24. (New) A transceiver module, comprising:

a ROSA;

a TOSA;

receive path eye opener circuitry including a first input and output and configured so that a first data stream received from the ROSA has a lower jitter at the first output than at the first input;

receive path bypass circuitry configured so that when the first data stream has a data rate less than about 10Gb/s, the first data stream bypasses the receive path eye opener circuitry along a first bypass path;

transmit path eye opener circuitry including a second input and output and configured so that a second data stream has a lower jitter at the second output than at the second input; and

transmit path bypass circuitry configured so that when the second data stream has a data rate less than about 10Gb/s, the second data stream bypasses the transmit path eye opener circuitry along a second bypass path, the second bypass path being in communication with the TOSA.

25. (New) The transceiver module as recited in claim 24, wherein the transceiver module is substantially compliant with the XFP MSA.

26. (New) The transceiver module as recited in claim 24, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs at a data rate of about 8.5Gb/s.

27. (New) The transceiver module as recited in claim 24, wherein at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises:

a CDR; and

a retimer.

28. (New) The transceiver module as recited in claim 24, wherein at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises one of: a passive equalization circuit; and, an active equalization circuit.

29. (New) The transceiver module as recited in claim 24, wherein the transmit path eye opener circuitry and the receive path eye opener circuitry are data rate responsive.

30. (New) The transceiver module as recited in claim 24, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry can be implemented in at least one of the following ways: manually; and, automatically.

31. (New) The transceiver module as recited in claim 24, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs for a range of data rates less than about 10Gb/s.

32. (New) The transceiver module as recited in claim 24, wherein:

the receive path eye opener circuitry and receive path bypass circuitry collectively comprise a receiver eye opener IC; and

the transmit path eye opener circuitry and transmit path bypass circuitry collectively comprise a transmitter eye opener IC.

33. (New) The transceiver module as recited in claim 32, wherein the receiver eye opener IC and transmitter eye opener IC each comprise circuitry for a plurality of eye openers, each of the plurality of eye openers being configured to operate in connection with a predetermined data rate or predetermined range of data rates.

34. (New) The transceiver module as recited in claim 24, wherein the transceiver module is compatible with the Fibre Channel protocol.

35. (New) A transceiver module, comprising:

a ROSA;

a TOSA;

receive path eye opener circuitry including a first input and output and configured so that a first serial data stream received from the ROSA has a lower jitter at the first output than at the first input;

receive path bypass circuitry configured so that when the first serial data stream has a data rate of about 8.5Gb/s, the first serial data stream bypasses the receive path eye opener circuitry along a first bypass path;

transmit path eye opener circuitry including a second input and output and configured so that a second serial data stream has a lower jitter at the second output than at the second input; and

transmit path bypass circuitry configured so that when the second serial data stream has a data rate of about 8.5Gb/s, the second serial data stream bypasses the transmit path eye opener circuitry along a second bypass path, the second bypass path being in communication with the TOSA,

and the transceiver module being substantially compliant with the XFP MSA.

36. (New) The transceiver module as recited in claim 35, wherein the transceiver module is compatible with the Fibre Channel protocol.

37. (New) The transceiver module as recited in claim 35, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry can be implemented in at least one of the following ways: manually; and, automatically.

38. (New) The transceiver module as recited in claim 35, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs for at least one other data rate in addition to the about 8.5Gb/s data rate.

39. (New) A transceiver module, comprising:
- a ROSA and a TOSA; and
 - a first IC configured to communicate with the ROSA, and a second IC configured to communicate with the TOSA, each IC configured to bypass clock and data recovery and retiming for a data rate of about 8.5Gb/s, and comprising:
 - a first buffer including a reference clock input and output;
 - a second buffer including data signal input and output, and an LOS output;
 - a CDR including:
 - a data signal input and output, the CDR data signal input connected to the second buffer data signal output;
 - reference clock input and output, the CDR reference clock input being connected to the first buffer reference clock output; and
 - an LOL output;
 - an RT including: a reference clock input connected to the CDR reference clock output; a data signal input connected to the CDR data signal output; and a data signal output;
 - a multiplexer including: a first input connected to the data signal output of the second buffer; a second input connected to the RT data signal output; a third input; and an output;
 - a third buffer including: an input connected to the multiplexer output; and an output; and
 - a control logic module including: a first input connected to the LOS output; a second input connected to the LOL output; a third input connectible to an external device; a first output connectible to an external device; and a second output connected to the third input of the multiplexer.

40. (New) The transceiver module as recited in claim 39, wherein:

the control logic module is responsive to:

an LOS signal from the second buffer;

an LOL signal from the CDR; and

a command from a host; and

the control logic module is configured to transmit a control signal to the multiplexer.

41. (New) The transceiver module as recited in claim 39, wherein the transceiver module is substantially compliant with the XFP MSA.

42. (New) The transceiver module as recited in claim 39, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs for at least one other data rate in addition to the about 8.5Gb/s data rate.

43. (New) The transceiver module as recited in claim 39, wherein the transceiver module is compatible with the Fibre Channel protocol.